Methodology for improved cell integration based on distributed-element circuit analysis

Gregory M. Kimball, Paola Murcia, Shefali Chandra, and Atiye Bayman

MiaSolé Hi-Tech Corp.

Santa Clara, California, United States.

***Abstract* – Improved cell integration is a critical part of narrowing the gap between cell and module efficiencies. In this paper, we present a methodology based distributed-element circuit analysis and electroluminescence imaging for optimizing the design of solar cell metallization and interconnection. The distributed-element circuit model is based on an array of equivalent circuits, each representing a 100x100 µm area of a thin film solar cell. A range of cell metallization designs are then compared within the simulation framework to deliver predictions of the effect of design changes on module efficiency. The optimized cell metallization design was tested experimentally on the manufacturing line, confirming the anticipated improvement in module efficiency. Distributed-element circuit analysis delivers reliable predictions of module efficiency and accelerates cell integration development projects.**

***Index Terms* – CIGS, distributed-element circuit analysis, electroluminescence, series resistance**

I. INTRODUCTION

The scale-up from research to manufacturing involves a dramatic increase in the sample area of solar devices. Although typical research cells have used a 1 cm^2 aperture area, manufactured solar modules are typically >1 m^2 in aperture area [1]. One of the major components of the gap between cell and module efficiencies is cell integration losses related to series resistance nonuniformity. Current collection in a solar device requires tradeoffs between shading losses due to opaque conductors and resistive loss in the positive and negative contacts. Previous work presented on all-PVD CIGS solar cells fabricated by MiaSolé showed that series resistance nonuniformity contributed a significant efficiency loss mechanism [2].

A variety of analytical and numerical approaches for optimizing resistive losses in solar cells have been described in the literature. The analytical approaches have delivered results in agreement with experiments, but typically employ simplified geometries [3]-[5]. Numerical methods have greater computational requirements, but are capable of capturing more complex geometries. The relationship of electroluminescence (EL) imaging and parasitic resistances has been explored in the literature, and allows for critical evaluation of circuit modeling results [6]. Distributed-element circuit analysis has been shown to accurately capture the behavior of parasitic resistances for thin film solar modules [7].

In this study, distributed-element circuit analysis was used to develop an improved cell integration design. Comparison with electroluminescence imaging was used to refine the circuit model, and a variety of modifications to cell integration geometry were evaluated. The most promising modification was validated experimentally and delivered the anticipated module efficiency improvement.

II. EXPERIMENTAL

The circuit modeling approach uses a distributed-element circuit model and represents the solar cell as an array of many thousands of passive circuit elements (Fig. 1a). Each modeling node is based on lumped circuit that contains a diode, current source, series resistor and parallel resistor, where the properties of each circuit element are estimated using IV data from individual solar cells. The modeling nodes connect into a mesh of series resistors representing the transparent conducting oxide layer (TCO) as well as the metallization layer. The circuits were subjected to DC analysis in NGSPICE. The discussion section contains additional details about determining the properties of the lumped circuit elements.

EL images were collected using Sensovation CoolSamBa HR830 silicon CCD. EL images were collected using two cycles of image acquisition and background subtraction, a measurement time of 20 sec, a constant current density of 30 mA/cm^2, and a resolution of 22 µm/pixel.

Fig. 1b shows a measured electroluminescence image collected from a subsection of a solar module. Fig. 1c shows a

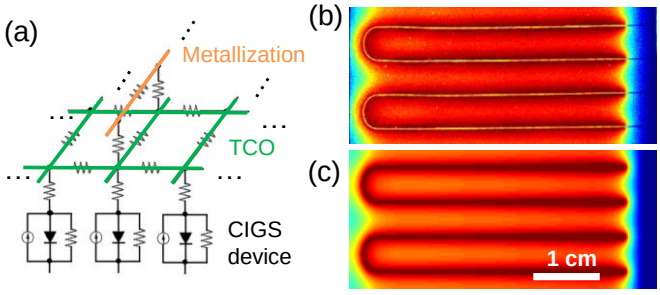


Fig. 1. (a) schematic of the distributed-element circuit analysis approach for optimizing metallization and TCO design. (b) Measured and (c) simulated electro-luminescence images from a solar cell of interest.

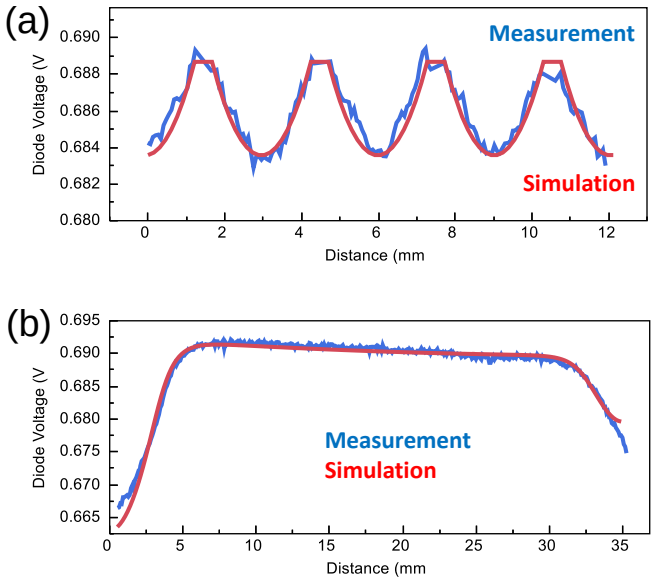


Fig. 2. Electroluminescence (EL) line scan overlays based on the images from Fig. 1b and 1c. Both (a) vertical and (b) horizontal EL line scans show the close correspondence between measurement and simulations.

simulated electroluminescence image obtained as part of DC operating analysis. The image was scaled from a map of local diode voltage by the following relation:

$$S_{EL} = \exp\left[\frac{(V_{diode} - c)}{kT/q}\right] \quad (1)$$

where S_{EL} is the signal intensity from EL, kT/q is the thermal voltage, and c is a proportionality constant set to 0.47 [2] [8]. The two images show highest voltage near the cell metallization, and decreasing voltage values further from the metallization due to voltage drop in the TCO layer.

Fig. 2 shows line scan data that was extracted from the two images, showing a correlation with $R^2 > 0.85$ across the two orthogonal device directions.

III. DATA AND RESULTS

Fig. 3 shows absolute module efficiency changes predicted from a series of cell integration geometries. In this case, "Metal to Edge" refers to the distance between the edge of the cell and the closest metallization feature. The model for baseline geometry was perturbed across a range of metal to edge distances for both cell edges. For each condition, module efficiency was determined from simulated light JV curves. The conclusion that smaller metal to edge distances have the highest performance was expected, but the circuit simulations provided the quantitative performance predictions needed to guide development work.

Fig. 4 shows EL imaging results from baseline and experimental cell integration designs that were selected based on the simulation results from Fig. 2. The expected improvement in EL intensity, marked by the black arrows, was

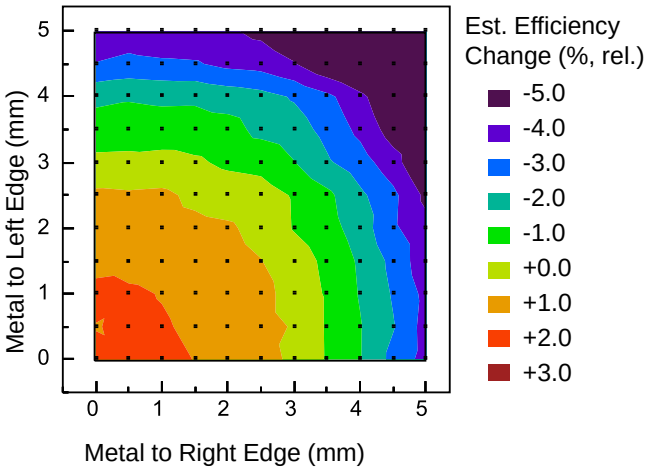


Fig. 3. Contour map showing simulation results for a range of cell integration geometries. The highest performance is expected for smaller "Metal to Edge" distances. "Left" and "Right" are based on the orientation of the solar cells shown in Fig. 1b,c.

observed at the "Right Edge" in accordance with circuit model simulation results.

Fig. 5 shows module performance results from a cell integration experiment conducted on the MiaSolé manufacturing line. An alternate cell integration design was compared to the baseline design for nominally identical device layers. Mean module Pmax difference was found to be +2.9 W, closely matching the predicted module performance difference of +2.7 W.

IV. DISCUSSION

The circuit model depicted in Fig. 1a is based on an array of equivalent circuits, each representing a small rectangular area

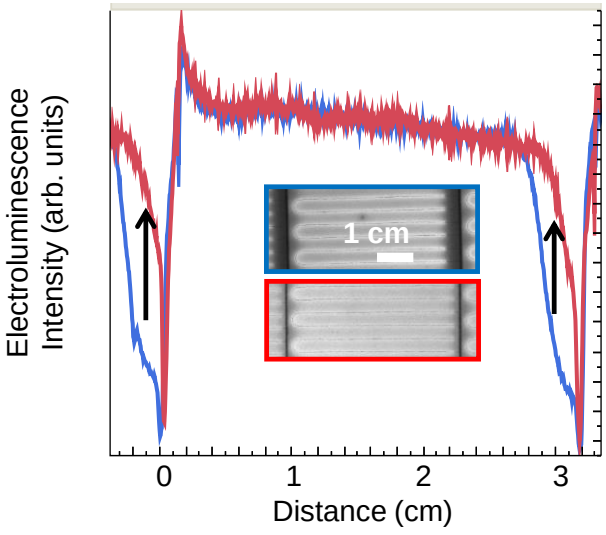
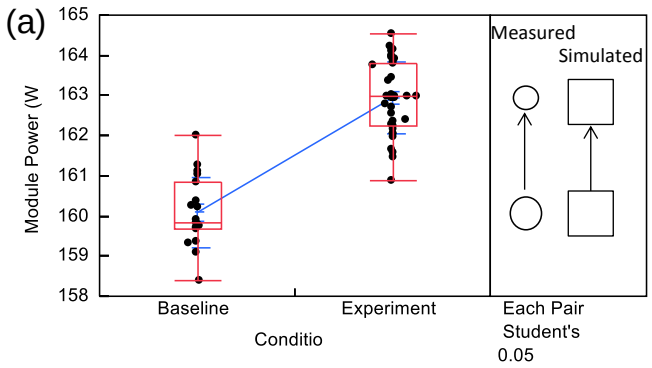


Fig. 4. Measured electroluminescence (EL) line scans and images from baseline (blue) and experimental (red) cell integration designs, where the experimental cell interconnect shows increased EL intensity at the cell edge.



(b)

Condition	Module Pmax (W)
Baseline	160.1 ± 0.9
Experiment	162.9 ± 0.9
Mean Difference	+2.9 W ± 0.3
Expected Difference	+2.7 W ± 0.7

Fig. 5. Module power results from the comparison of baseline and experimental cell interconnect designs. Experimental cell interconnect design shows +2.9 W (+1.8% relative) mean module power improvement.

of a thin film solar cell. A single metallization loop was used with periodic boundary conditions to represent the contribution of adjacent loops. The metallization features fill the area of a modeling node only fractionally, so the resistance values to adjacent nodes were scaled based on the fraction of metallization making contact to each adjacent node. Shading losses were implemented by reducing the current source elements by the fractional metallization coverage.

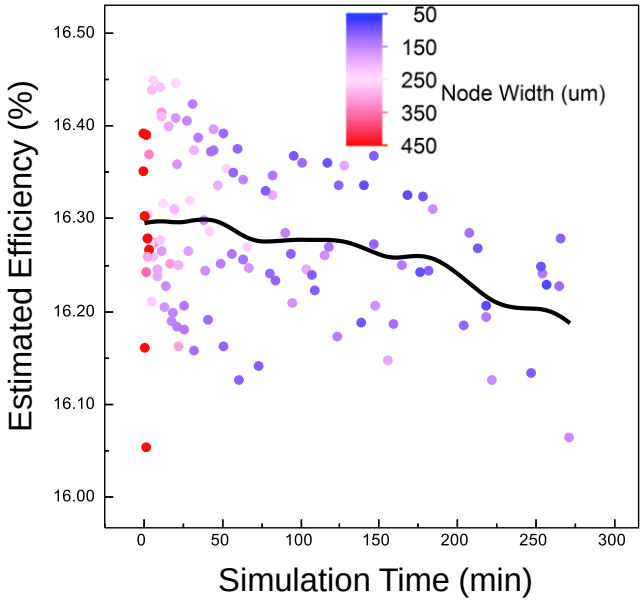


Fig. 6. Scatter plot showing estimated device efficiency results for a range of simulation node width values. The standard deviation in estimated device efficiency is found to decrease with smaller node size. Simulations with node width values <200 µm were found to provide efficiency estimates with a standard deviation value <0.05% abs.

The TCO resistors in the vertical and horizontal axes were computed based on the aspect ratio of each modeling node. Contact resistance between the metallization and the TCO and sheet resistance of the substrate were both neglected. The device layer circuit element properties were estimated from ideal diode fits to JV characteristics of small-area solar cells. Circuit files were generated programmatically with typical node dimensions of 150x150 µm, and 20K to 100K elements per simulation.

The relationship between the simulation node dimensions and the estimated efficiency showed only weak dependence. Fig. 6 shows the results from a series of simulations using different numbers of simulation nodes for the same cell design. Although essentially all of the results fall within an efficiency window of ± 0.1% abs., there is a decrease in both the simulated device efficiency and the standard deviation of device efficiency estimates as the node size is decreased. The reduction in estimated efficiency with decreasing node size is likely related to the smaller effect of TCO sheet resistance in when the node size is much bigger than the metallization dimensions. Simulations with node width values <200 µm were found to provide a standard deviation in efficiency that was <0.05% abs.

The estimated efficiency changes depicted in Fig. 2 are mainly driven by FF effects, as would be expected for changes in series resistance losses. The strong FF trend hides a smaller loss in Jsc for reduced "Metal to Left Edge" spacing due to increased metallization shading loss. In this case, there is no expected benefit in efficiency for positioning the metallization further from cell edge.

Although the distributed-element circuit analysis was applied to a few metallization variables in this case, it can also be applied to a wide variety of device optimization projects. The tradeoff of TCO sheet resistance and free carrier absorption, alternate approaches to metallization, and cell dimensions are other cell integration topics well-suited to exploration with distributed-element circuit analysis. Simulation results can explore variables that are difficult to change, such as cell dimensions, and also allows for co-optimization of many parameters, such as metallization geometry for alternate cell dimensions. In this way, distributed-element circuit analysis accelerates development projects in cell integration and focuses resources on the most promising designs.

V. SUMMARY

A distributed-element circuit model was developed for studying resistive losses in thin film solar cells. The model was validated using the comparison between measured and simulated electroluminescence imaging. Simulation results were presented to show the expected module performance across a series of metallization designs, and experimental results were presented demonstrating the expected performance improvement.

REFERENCES

[1] M. A. Green, K. Emery, Y. Hishikawa, W. Warta and E. D. Dunlop, "Solar cell efficiency tables (Version 45)," *Progress in Photovoltaics,* vol. 23, pp. 1-9, 2015.

[2] G. M. Kimball, N. Mackie, M. Parker and A. Bayman, "Evaluation of Micro- and Nanoscale Uniformity in All-PVD Cu(In,Ga)Se2 Solar Cells," *Conference Record of the Fortieth IEEE Photovoltaic Specialists Conference,* 2014.

[3] P. P. Altermatt, G. Heiser, A. G. Aberle, A. Wang, J. Zhao, S. J. Robinson, S. Bowden and M. A. Green, "Spatially Resolved Analysis and Minimization of Resistive Losses in High-efficiency Si Solar Cells," *Progress in Photovoltaics,* vol. 4, pp. 399-414, 1996.

[4] A. Antonini, M. Stefancich, D. Vincenzi, C. Malagu, F. Bizzi, A. Ronzoni and G. Martinelli, "Contact grid optimization methodology for front contact concentrator solar cells," *Solar Energy Materials & Solar Cells,* vol. 80, pp. 155-166, 2003.

[5] A. R. Burgers, "How to Design Optimal Metallization Patterns for Solar Cells," *Progress in Photovoltaics,* vol. 7, pp. 457-461, 1999.

[6] A. Helbig, T. Kirchartz, R. Schaeffler, J. Werner and U. Rau, "Quantitative electroluminescence analysis of resistive losses in Cu(In,Ga)Se2 thin-film modules," *Solar Energy Materials & Solar Cells,* vol. 94, pp. 979-984, 2010.

[7] G. Brown, A. Pudov, B. Cardozo, V. Faifer, E. Bykov and M. Contreras, "Quantitative imaging of electronic nonuniformities in Cu(In,Ga)Se2 solar cells," *Journal of Applied Physics,* vol. 108, p. 074516, 2010.

[8] U. Rau, "Reciprocy relation between photovoltaic quantum efficiency and electroluminescent emission of solar cells," *Physical Review B,* vol. 76, p. 085303, 2007.